

REMARKS

The following remarks are submitted in response to the outstanding Office Action wherein the Examiner rejected Claims 1-13, all the claims under consideration. Reconsideration and allowance of the application in view of the following remarks is respectfully requested.

Prior to discussing the prior art rejections, Applicants take this opportunity to set forth the following brief remarks about the claimed invention. Applicants' invention utilizes a stacked gate structure to control the stress produced in the channel of the device, wherein the stacked gate structures includes a gate dielectric, a first stressed film layer of large grain size Si or SiGe formed on top of a gate dielectric layer, and a second stressed film layer of strained SiGe or strained Si:C formed on top the first stressed film layer, as recited in Claim 1. Applicants' claimed gate structure produces stresses in the channel of the device. The applied references fail to teach or suggest at least these required features of Applicants' claims.

In the present Official Action, Claims 1 and 2 are rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent Application Publication No. 2004/0108559A1 to Suggii et al. ("Suggii et al."). Claims 3-13 stand rejected, under 35 U.S.C. 103(a), as allegedly being unpatentable over Suggii et al. in view of U.S. Patent Application Publication No. 2005/0189589 to Zhu et al. ("Zhu et al."). Applicants respectfully disagree and submit the following.

Turning first to the §102 rejection of Claims 1 and 2, Applicants note that Suggii et al. fail to disclose a stacked gate structure of SiGe and/or Si:C that produces stress in the channel region of the transistor device that is positioned beneath the stacked gate structure of SSi(strained Si)/SiGe or SSi/Si:C, as recited in Claim 1. Applicants note that there is no suggestion, teaching or reference in the Suggii et al. disclosure of a gate structure of stacked gate conductors or

teaching of where a gate structure produces a stress in the channel of a transistor device. Suggii et al. merely teaches a conventional gate composed of single gate electrode (see reference number 8 in Figure 4B), wherein the single gate electrode is separated from the channel by a gate insulator. (see reference number 7 in Figure 4B).

Referring to Pages 2 and 3 of the present Office Action, the Examiner alleges that Figures 1-9 and paragraphs 103-104 of the Suggii et al. disclosure meet the limitation of Applicants' claimed gate structure, since Figures 1-9 allegedly depict a stacked gate region including SiGe, strained Si, an oxide layer and a polysilicon gate. Applicants respectfully disagree.

Applicants submit that the SiGe layer (reference number 4 of the Suggii et al. reference) and strained Si (reference number 3 of the Suggii et al. reference), which is being referred to by the Examiner in the present §102 rejection of Claims 1 and 2, are components of the substrate that is disclosed in the Suggii et al. reference, which is not the gate structure and is in fact the channel of the device. The channel of the device is positioned in the substrate underlying the gate dielectric and separates the source region from the drain region of the field effect transistor. Referring to paragraph 0104 of the Suggii et al. disclosure, Suggii et al. further describe the substrate as follows:

"The strained silicon/strain-relaxed silicon germanium substrate shown in FIG. 1 is first prepared. Herein, a substrate having at least strained silicon layer/strain-relaxed silicon germanium layer, in the upper part of a silicon substrate, is called "strained silicon/strain-relaxed silicon germanium substrate". This substrate can be fabricated by forming a strain-relaxed silicon germanium layer 2, a strained silicon layer 3, a strain-relaxed silicon germanium layer 4, and a strained silicon layer 5, in that order, on top of a conventional silicon substrate 1, by use of a conventional epitaxial growth method."

Suggii et al. utilize layers of SiGe and silicon in the channel region of the device, which is underlying the gate dielectric and the gate conductor to produce a strain in the channel. Suggii et

al. fail to teach or suggest a stacked gate structure including a first stressed film layer of large grain size Si or SiGe formed on top of a gate dielectric layer, and a second stressed film layer of strained SiGe or strained Si:C formed on top the first stressed film layer, and that the stacked gate structure of SiGe and/or Si:C produces stresses in the channel region of the transistor, as required by Claim 1.

Therefore, since Suggii et al. fail to disclose each and every limitation of Claim 1, Applicants respectfully submit that the instant §102 rejections has been obviated and withdrawal thereof is respectfully requested. Furthermore, the §102(e) rejection of Claim 2 is improper since each of these claims depend from Claim 1, which is not anticipated by Suggii et al. as demonstrated herein.

Turning to the §103 rejection of Claims 3-13, Applicants submit that Zhu et al. is disqualified as a reference. The statute under 35 U.S.C. §103(c) states that:

Subject matter developed by another person, which qualifies as prior art only under one or more subsections (e), (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Applicants submit that the Zhu et al. reference was applied by the Examiner as prior art under 35 U.S.C. §103 via 35 U.S.C. §102(e). Applicants note in this regard that MPEP §706.02(k) states that:

Effective November 29, 1999, subject matter which was prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e) is now disqualified as prior art against the claimed invention if that subject matter and the claimed invention “were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.”

In view of the above, and the fact the present application and Zhu et al. "were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person", the Zhu et al. reference is disqualified as a reference under 35 U.S.C. §103(c).

To evidence that the instant application and Zhu et al. "were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person", the assignment document of the present application (recordation date April 23, 2004 at Reel 014525, Frame 0620) was compared with the recorded assignment of Zhu et al. (recordation date February 27, 2004 at Reel 014371, Frame 0604). In both instances, the inventors conveyed their entire interest to International Business Machines Corporation; therefore establishing common ownership between the instant application and the applied Zhu et al.

In view of the above information, Zhu et al. is disqualified as art and the instant §103 rejection is also solely based on Suggii et al. Applicants submit, in this regard, that Suggii et al. by itself does not anticipate, or render obvious, the claimed invention as discussed above. Thus, the rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

In view of the foregoing, this application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call Applicant's attorney at (516) 742-4343.

Respectfully submitted,



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